

Appl. No. 10/690,859  
Examiner: LE, THAO P, Art Unit 2818  
In response to the Office Action dated February 23, 2005

Date: May 23, 2005  
Attorney Docket No. 10113101

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims

**Claim 1 (Currently Amended):** A method for forming a trench isolation, comprising:  
providing a semiconductor substrate with a trench, wherein the semiconductor substrate has a mask layer;  
~~conformably forming a first insulating layer~~ LPCVD oxide layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the ~~first insulating layer~~ LPCVD oxide layer;  
anisotropically etching the ~~first insulating layer~~ LPCVD oxide layer to below the level of the semiconductor substrate;  
forming a ~~second~~ an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench; and  
planarizing the ~~second~~ insulating layer to expose the mask layer.

**Claim 2 (Original):** The method for forming a trench isolation as claimed in claim 1, wherein the mask layer is a nitride layer.

**Claims 3-4 (Canceled)**

**Claim 5 (Original):** The method for forming a trench isolation as claimed in claim 1, wherein the anisotropic etching is plasma etching or reactive ion etching.

**Claim 6 (Currently Amended):** The method for forming a trench isolation as claimed in claim 1, wherein the ~~first insulating layer~~ LPCVD oxide layer is lower than the semiconductor substrate by at least 300Å after anisotropic etching.

**Claim 7 (Currently Amended):** The method for forming a trench isolation as claimed in claim 1, wherein the ~~second~~ insulating layer is an oxide layer.

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**Claim 8 (Original):** The method for forming a trench isolation as claimed in claim 7, wherein the oxide layer is a TEOS oxide layer.

**Claim 9 (Original):** The method for forming a trench isolation as claimed in claim 1, wherein the planarizing is chemical mechanical polishing.

**Claim 10 (Currently Amended):** A method for forming a trench isolation, comprising:  
providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with an opening are sequentially formed thereon;  
sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a trench using the patterned photoresist layer as a mask;  
removing the patterned photoresist layer;  
conformably forming an LPCVD oxide layer to cover the semiconductor substrate and the trench, wherein the trench is filled with the LPCVD oxide layer;  
anisotropically etching the LPCVD oxide layer to lower its surface below a top surface of the semiconductor substrate by at least 300Å;  
forming an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench, wherein the trench is filled with the insulating layer;  
planarizing the insulating layer to expose the mask layer; and  
removing the mask layer.

**Claim 11 (Original):** The method for forming a trench isolation as claimed in claim 10, wherein the pad layer is an oxide layer.

**Claim 12 (Original):** The method for forming a trench isolation as claimed in claim 10, wherein the mask layer is a nitride layer.

**Claim 13 (Original):** The method for forming a trench isolation as claimed in claim 10, wherein the aspect ratio of the trench is greater than 6.

**Claim 14 (Original):** The method for forming a trench isolation as claimed in claim 10, wherein the anisotropic etching is plasma etching or reactive ion etching.

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**Claim 15 (Original):** The method for forming a trench isolation as claimed in claim 10, wherein the insulating layer is an oxide layer.

**Claim 16 (Original):** The method for forming a trench isolation as claimed in claim 15, wherein the oxide layer is a TEOS oxide layer.

**Claim 17 (Original):** The method for forming a trench isolation as claimed in claim 10, wherein the planarizing is a chemical mechanical polishing.

**Claim 18 (Currently Amended):** A method for forming a trench isolation, comprising:  
providing a semiconductor substrate with a trench, wherein the semiconductor substrate has a mask layer;  
forming a first insulating layer LPCVD oxide layer to cover the semiconductor substrate and the trench;  
anisotropically etching the first insulating layer LPCVD oxide layer to form a spacer on a sidewall of the trench;  
forming a second an insulating layer to cover the semiconductor substrate and the LPCVD oxide layer in the trench; and  
planarizing the second insulating layer to expose the mask layer.

**Claim 19 (Original):** The method for forming a trench isolation as claimed in claim 18, wherein the mask layer is a nitride layer.

**Claims 20-21 (Canceled)**

**Claim 22 (Original):** The method for forming a trench isolation as claimed in claim 18, wherein the anisotropic etching is plasma etching or reactive ion etching.

**Claim 23 (Original):** The method for forming a trench isolation as claimed in claim 18, wherein the spacer is lower than the semiconductor substrate.

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**Claim 24 (Currently Amended): The method for forming a trench isolation as claimed in claim 18, wherein the second insulating layer is an oxide layer.**

**Claim 25 (Original): The method for forming a trench isolation as claimed in claim 24, wherein the oxide layer is a TEOS oxide layer.**

**Claim 26 (Original): The method for forming a trench isolation as claimed in claim 18, wherein the planarizing is chemical mechanical polishing.**

**Claim 27 (Currently Amended): A method for forming a trench isolation, comprising:**

providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with an opening are sequentially formed thereon;

sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a trench using the patterned photoresist layer as a mask;

removing the patterned photoresist layer;

conformably forming an LPCVD oxide layer to cover the semiconductor substrate and the trench;

anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the trench;

forming an insulating layer to cover the semiconductor substrate and LPCVD oxide layer in the trench;

planarizing the insulating layer to expose the mask layer; and

removing the mask layer.

**Claim 28 (Original): The method for forming a trench isolation as claimed in claim 27, wherein the pad layer is an oxide layer.**

**Claim 29 (Original): The method for forming a trench isolation as claimed in claim 27, wherein the mask layer is a nitride layer.**

**Claim 30 (Original): The method for forming a trench isolation as claimed in claim 27, wherein the aspect ratio of the trench is greater than 6.**

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**Claim 31 (Original):** The method for forming a trench isolation as claimed in claim 27, wherein the anisotropic etching is plasma etching or reactive ion etching.

**Claim 32 (Original):** The method for forming a trench isolation as claimed in claim 27, wherein the spacer is lower than the semiconductor substrate.

**Claim 33 (Original):** The method for forming a trench isolation as claimed in claim 27, wherein the insulating layer is an oxide layer.

**Claim 34 (Original):** The method for forming a trench isolation as claimed in claim 33, wherein the insulating layer is a TEOS oxide layer.

**Claim 35 (Original):** The method for forming a trench isolation as claimed in claim 27, wherein the planarizing is performed by chemical mechanical polishing.

**Claim 36 (Currently Amended):** A method for forming a trench isolation, comprising:  
providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with a first opening and a second opening are sequentially formed thereon;  
sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a first trench and a second trench using the patterned photoresist layer as a mask, wherein the aspect ratio of the first trench is greater than 6;  
removing the patterned photoresist layer;  
conformably forming an LPCVD oxide layer to cover the semiconductor substrate, the first trench, and the second trench, wherein the first trench is filled with the LPCVD oxide layer;  
anisotropically etching the LPCVD oxide layer to lower its surface below a top surface of the semiconductor substrate by at least 300Å;  
forming an insulating layer to cover the semiconductor substrate, the LPCVD oxide layer in the first trench and the LPCVD oxide layer in the second trench, wherein the first trench and the second trench are filled with the insulating layer;

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planarizing the insulating layer to expose the mask layer; and  
removing the mask layer.

**Claim 37 (Original):** The method for forming a trench isolation as claimed in claim 36, wherein the pad layer is an oxide layer.

**Claim 38 (Original):** The method for forming a trench isolation as claimed in claim 36, wherein the mask layer is a nitride layer.

**Claim 39 (Original):** The method for forming a trench isolation as claimed in claim 36, wherein the anisotropic etching is plasma etching or reactive ion etching.

**Claim 40 (Original):** The method for forming a trench isolation as claimed in claim 36, wherein the insulating layer is a TEOS oxide layer.

**Claim 41 (Original):** The method for forming a trench isolation as claimed in claim 36, wherein the planarizing is performed by chemical mechanical polishing.

**Claim 42 (Currently Amended):** A method for forming a trench isolation, comprising:  
providing a semiconductor substrate, wherein a pad layer, a mask layer, and a patterned photoresist layer with a first opening and a second opening are sequentially formed thereon;  
sequentially etching the mask layer, the pad layer, and the semiconductor substrate to form a first trench and a second trench using the patterned photoresist layer as a mask, wherein the aspect ratio of the first trench is greater than 6;  
removing the patterned photoresist layer;  
conformably forming an LPCVD oxide layer to cover the semiconductor substrate;  
anisotropically etching the LPCVD oxide layer to form a spacer on a sidewall of the first trench;  
forming an insulating layer to cover the semiconductor substrate, the LPCVD oxide layer in the first trench and the LPCVD oxide layer in the second trench;

planarizing the insulating layer to expose the mask layer; and

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removing the mask layer.

**Claim 43 (Original):** The method for forming a trench isolation as claimed in claim 42, wherein the pad layer is an oxide layer.

**Claim 44 (Original):** The method for forming a trench isolation as claimed in claim 42, wherein the mask layer is a nitride layer.

**Claim 45 (Original):** The method for forming a trench Isolation as claimed in claim 42, wherein the anisotropic etching is plasma etching or reactive ion etching.

**Claim 46 (Original):** The method for forming a trench isolation as claimed in claim 42, wherein the spacer is lower than the semiconductor substrate.

**Claim 47 (Original):** The method for forming a trench isolation as claimed in claim 42, wherein the insulating layer is a TEOS oxide layer.

**Claim 48 (Original):** The method for forming a trench isolation as claimed in claim 36, wherein the planarizing is chemical mechanical polishing